WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate;

an insulating film formed on the substrate;

a first semiconductor layer lattice-relaxed and formed on the insulating film substantially in contact therewith;

a second semiconductor layer having a tensile lattice strain and formed on the first semiconductor layer, a lattice constant of the second semiconductor layer being smaller than that of the first semiconductor layer;

a gate insulting layer selectively formed on the second semiconductor layer;

a gate electrode formed on the gate insulating film;

a channel region formed in a surface of the second semiconductor layer immediately under the gate electrode; and

a pair of source/drain regions selectively formed in the second semiconductor layer so as to be spaced apart from each other by the channel region.

2. The semiconductor device according to claim 1, wherein a thickness of the first semiconductor layer is 80 nm or less.

3. The semiconductor device according to claim 1, wherein a total thickness of the first semiconductor

layer and the second semiconductor layer is made to be 100 nm or less.

4. The semiconductor device according to claim 1, wherein a lattice distance of the first semiconductor layer is varied in a thickness direction.

5. The semiconductor device according to claim 1, wherein the first semiconductor layer is an SiGe layer having a Ge content at a part thereof adjacent to the second semiconductor layer at least larger than 30 atomic %, and the second semiconductor layer is an Si layer.

6. The semiconductor device according to claim 1, wherein the first semiconductor layer is an SiGe layer having a gradient content of Ge in a thickness direction, a Ge content of the first semiconductor layer at a portion thereof adjacent to the base substrate being 30 atomic % or less and a Ge content of the first semiconductor layer at a portion thereof adjacent to the second semiconductor layer being larger than 30 atomic %; and the second semiconductor layer is Si.

7. The semiconductor device according to claim 1, wherein the first semiconductor layer and the second semiconductor layer are different in lattice constant and a combination selected from the group consisting of Si, SiGe, GaAs, SiC, GaN, GaAlAs, InGaP, InGaPAs, Al_2O_3, Bn, BNC, C, doped Si, SiNx, and ZnSe to apply

a tensile strain to the first semiconductor layer.

8. A method of manufacturing a semiconductor device comprising:

a first step of forming an insulating film on a substrate;

a second step of forming a stacked substrate having a stacked layer of a first semiconductor layer and a second semiconductor formed on the first semiconductor layer;

a third step of bonding the substrate and the stacked substrate such that the insulating film faces the first semiconductor layer;

a forth step of removing the stacked substrate so as to allow the first semiconductor layer and at least part of the second semiconductor layer to remain, thereby forming a stacked structure formed of the first semiconductor layer lattice-relaxed and the second semiconductor layer having a strain applied on a surface thereof; and

a fifth step of forming a transistor on the second semiconductor layer having the strain applied on the surface thereof.

9. The method according to claim 8, wherein the fifth step includes the steps of:

forming a gate insulating film selectively on an upper surface of the second semiconductor layer;

doping impurities for forming a channel region

into an upper surface of the second semiconductor layer immediately under the gate insulating film;

forming a gate electrode on the gate insulating film; and

doping impurities selectively into the second semiconductor layer along opposite sides of the gate electrode with the gate electrode used as a mask, thereby forming a pair of source/drain regions.

10. The method according to claim 8, wherein the second step includes a step of controlling a thickness of the first semiconductor layer to 80 nm or less.

11. The method according to claim 8, wherein the fourth step includes a step of controlling a total thickness of the first semiconductor layer and the at least part of the second semiconductor layer to 100 nm or less.

12. The method according to claim 8, wherein the second step includes a step of forming the first semiconductor layer while varying a lattice distance in a film-thickness direction.

13. The method according to claim 8, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer, respectively, and the second step includes a step of controlling a Ge content of the first semiconductor layer at least at a portion thereof adjacent to the second semiconductor layer at more than 30 atomic %.

14. The method according to claim 8, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer, respectively, and the second step include a step of controlling a Ge content to have a gradient content in such a manner that a Ge content of a portion of the first semiconductor layer adjacent to the insulating layer is set at 30% or less and a Ge content of a portion of the first semiconductor layer adjacent to the second semiconductor layer is set at more than 30 atomic %.

15. A method of manufacturing a semiconductor device comprising:

a first step of forming an insulating film on a substrate;

a second step of forming a first semiconductor layer on a surface of a semiconductor substrate;

a third step of bonding the substrate and the semiconductor substrate such that the insulating film faces the first semiconductor layer;

a forth step of removing the semiconductor substrate so as to leave at least the first semiconductor layer, thereby lattice-relaxing the first semiconductor layer;

a fifth step of stacking a second semiconductor layer on the first semiconductor layer, thereby applying a tensile strain to the second semiconductor layer; and

a sixth step of forming a transistor on the second semiconductor layer.

16. The method according to claim 15, wherein the sixth step includes the steps of:

forming a gate insulating film selectively on an upper surface of the second semiconductor layer;

doping impurities for forming a channel region into an upper surface of the second semiconductor layer immediately under the gate insulating film;

forming a gate electrode on the gate insulating film; and

forming a pair of source/drain regions by doping impurities selectively in the second semiconductor film along opposite sides of the gate electrode with the gate electrode used as a mask.

17. The method according to claim 15, wherein the fourth step includes a step of controlling a thickness of the first semiconductor left to 80 nm or less.

18. The method according to claim 15, wherein the fifth step includes a step of controlling a total thickness of the first semiconductor layer and the second semiconductor layer to 100 nm or less.

19. The method according to claim 15, wherein the second step includes a step of varying a lattice distance of the first semiconductor layer in a film thickness direction.

20. The method according to claim 15, wherein the

first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer and the second step includes a step of setting a Ge content of a part of the first semiconductor layer at least adjacent to the second semiconductor layer at more than 30 atomic %.

21. The method according to claim 15, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer, respectively, and the fourth step includes a step of controlling a Ge content to have a gradient content in such a manner that a Ge content of the first semiconductor layer a portion thereof adjacent to the insulating layer is set at 30 atomic % or less and a Ge content of a surface of the first semiconductor layer exposed to air is set at more than 30 atomic %.

22. A semiconductor substrate comprising:

a substrate;

an insulating film formed on the substrate;

a first semiconductor layer lattice-relaxed formed on the insulating film; and

a second semiconductor layer formed on the first semiconductor layer and having a tensile lattice strain.